AMENDMENTS TO THE CLAIMS

1-4. (Cancelled)

5. (Currently Amended) An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area;

wherein each of the MOS FETs has a source region of the first conductivity type, [[coupled]] directly connected to a power rail.

6. (Currently Amended) An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area;

wherein the first well is [[coupled]] electrically connected to a pad through the extension areas.

7. (Currently Amended) An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area;

wherein the first doping region is [coupled] directly connected to a pad.

8. (Currently Amended) An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type; and

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area;

wherein each of the MOS FETs has a drain region of the first conductivity type, [coupled] directly connected to a pad.

9. (Currently Amended) An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, comprising:

two gates, formed in parallel on a first semiconductive layer having a second conductivity type;

two sources of the first conductivity type, directly connected [[coupled]] to a power supply; and

two drains of the first conductivity type;

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area, and [[coupled]] directly connected to a pad; and

a guard ring of the second conductivity type, formed on the first semiconductive layer, [[coupled]] directly connected to the power supply;

wherein the first well is [[coupled]] electrically connected to the pad through the extension areas.